8/15/03
#12 (Appeal Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Hung Yip Ng

Serial No.: 09/821,478 **Group Art Unit:** 1756

Filed: March 29, 2001 **Examiner:** Sagar, Kripa

For: METHOD FOR POLYSILICON CONDUCTOR (PC) TRIMMING FOR SHRINKING CRITICAL DIMENSION AND ISOLATED-NESTED OFFSET CORRECTION

Honorable Commissioner of Patents
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BRIEF ON APPEAL

Appeal from Group 1700

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I. REAL PARTY IN INTEREST

The real party in interest for this appeal and the present application are International Business Machines Corporation by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 011705, Frame 0794.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences, known to the Appellants, the Appellants' representatives or the Assignee, which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Applicants appeal the final rejection of claims 1, 3-8, 10-14 and 16-20. No other claims are pending.

IV. STATUS OF AMENDMENTS

An Amendment After Final Rejection was filed on April 16, 2003. By an Advisory Action mailed May 2, 2003, the Examiner indicated that the Amendment would be entered upon filing of a Notice of Appeal and an Appeal Brief.

V. SUMMARY OF INVENTION

The claimed invention is directed to a method of forming a semiconductor device including lithographically patterning a structure having a first critical dimension and etching the structure. The structure includes nested features and an isolated feature. The etching is

performed with an O2-containing material to trim the first critical dimension to a second critical dimension which is smaller than the first critical dimension. The etching corrects an offset between the nested features and the isolated feature which were created during the lithographic patterning.

Conventional semiconductor devices have suffered from nested and isolated feature offset which resulted from the lithographic process which created those features. In other words, conventional lithographic techniques for forming structures have limitations which create an offset between nested and isolated features. For example, lithographic processes have optical properties of light reflection which may adversely affect the isolated/nested offset. Therefore, prior to the present invention, no suitable method has existed for defining the gate dimension before the gate etching (page 4, lines 19-20).

The present invention lithographically forms a structure which includes nested and isolated features and subsequently corrects for the isolated/nested offset from the lithographic formation by etching with an O2 containing material. Specifically, the present invention controls the etching such that any offset which was caused by a lithographic process is corrected. In other words, the present invention corrects for the isolated/nested offset from the previous lithographic formation by etching, as opposed to etching to correct for any isolated nested offset which would otherwise result from a subsequent lithographic formation.

VI. ISSUE

Whether claims 1, 3-8, 10-14 and 16-20 are unpatentable under 35 U.S.C. § 103 over Tao et al. in view of Ma et al. and further in view of Horak et al.

VII. GROUPING OF CLAIMS

There are four groups of claims: Group I - claims 1, 3-7; Group II - claims 8, 10-13; Group III - claims 14 and 16-18; and Group IV - claims 19-20. The groups do not stand or fall together. Claims 3-7 stand or fall together with claim 1. Claims 10-13 stand or fall together with claim 8. Claims 16-18 stand or fall together with claim 14. Claim 20 stands or falls together with claim 19.

Claim 1 is directed to an exemplary embodiment of the present invention. Claim 1 recites "*[a] method of forming a semiconductor device, comprising:*

lithographically patterning a structure having a first critical dimension, wherein said structure includes nested features and an isolated feature;

etching said structure with an O2-containing material to trim said first critical dimension to a second critical dimension to correct an offset between said nested features and said isolated feature created by said lithographic patterning."

Claim 8 recites similar subject matter to claim 1. However, unlike independent claim 1, claim 8 recites "*said second critical dimension being smaller than said first critical dimension.*"

Claim 14 is directed to another exemplary embodiment of the present invention. Claim 14 recites "*[a] method of etching a semiconductor device, comprising:*

lithographically forming nested features and an isolated feature; and

etching said semiconductor device using a surface charging technique in combination with a plasma etch, such that a nested features formed on said semiconductor device are etched faster than an isolated feature formed on said semiconductor device to compensate for an offset between said nested features and said isolated features which resulted from said

lithographic formation of said nested features and said isolated features."

Claim 19 recites similar subject matter to claim 14. However, unlike independent claim 14, claim 19 recites "*wherein said nested features and said isolated feature comprises a negative photoresist.*"

In addition, each of the dependent claims is patentably distinct from the independent claim from which it depends. More specifically, claims 3-7, 10-13, 16-18 and 20 are patentably distinct from their respective independent claims.

Each dependent claim recites additional features, not defined in the respective independent claim. The features recited by the dependent claims are not merely illustrations or examples, but are patentable features.

VIII. ARGUMENT

A. The Tao et al., Ma et al. and Horak et al. references would not have been combined by one of ordinary skill in the art at the time of the invention.

To establish obviousness under 35 U.S.C. § 103, the Examiner must show that the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention was made to a person having ordinary skill in the art to which the subject matter pertains. In re Reuter, 651 F.2d 751, 210 USPQ 249 (CCPA 1981). However, obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention without a teaching, suggestion or motivation to support the combination. ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

The Examiner alleges that the Ma et al. reference would have been combined with the

Tao et al. reference and further that the Horak et al. reference would have been combined with the combination of the Ma et al. and the Tao et al. references to form the claimed invention. Applicant submits, however, that these references would not have been combined.

Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the Tao et al. reference is directed to forming a very narrow polysilicon gate line (col. 1, lines 65-67) using a consumable hard mask of silicon oxynitride covered by a thin layer of silicon oxide during the etching of the polysilicon (col. 2, lines 6-9). The Tao et al. reference combines the functions of the anti-reflection coating function and the substitution of a hard mask during the etching step (col. 2, lines 8-12).

In contrast, the Ma et al. reference is specifically directed to reducing a power frequency in a plasma etch reactor so that the plasma source power level may be increased which provides complete residue removal and prevents etch microloading (col. 3, lines 10-28). The Ma et al. reference is not concerned with the problem of forming a very narrow polysilicon gate line as disclosed by the Tao et al. reference. Rather, the Ma et al. reference is concerned with the completely different problem of reducing a power frequency in a plasma etch reactor. Therefore, one of ordinary skill in the art would not have referred to the Ma et al. reference when attempting to solve the problem of forming a very narrow polysilicon gate line as disclosed by the Tao et al. reference. Thus, the Tao et al. and Ma et al. references would not have been combined, absent hindsight.

Further, the Horak et al. reference is specifically directed to performing a reactive ion etching process which compensates for a subsequent normal etching process to prevent a

nested/isolated feature offset (col. 6, line 49 - col. 7, line 2). The Ma et al. reference teaches entirely avoiding any such "profile microloading." Therefore, one of ordinary skill in the art would not have been motivated to modify the teachings of the Ma et al. reference with a reactive ion etching process which compensates for a subsequent etching process as disclosed by the Horak et al. reference because the Ma et al. reference discloses a method which entirely avoids any such problem. Therefore, the references would not have been combined, absent hindsight.

B. The Tao et al., Ma et al. and Horak et al. references do not teach or suggest each and every element of the claimed combination.

Even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention. The present invention recites etching a structure to correct an offset between isolated and nested structures which were created by a lithographic process. As explained above, this feature is important for correcting offsets which were created as a result of the optical characteristics of the lithographic process.

In other words, the present invention corrects for the isolated/nested offset from the previous lithographic formation, as opposed to correcting for any isolated nested offset which would otherwise result from a subsequent lithographic formation.

For example, as shown in Figs 2A and 2B, the present invention may involve lithographically patterning the resist pattern 203 having a first critical dimension CD1 and then etching the resist pattern 203 to trim the first critical dimension CD1 to a second critical dimension CD2 to correct an offset in the resist pattern 203.

The Tao et al. reference does not teach anything at all about isolated/nested offset, let alone any such offsets which are created during lithographic processing. Indeed, the Examiner admits that the Tao et al. reference "does not teach correcting for the CD-bias" (page 4, line 1). However, contrary to the Examiner's allegations, the remaining references do not remedy the deficiencies of the Tao et al. reference.

The Ma et al. reference discloses that "profile microloading" may occur during an etching as a result of etch-by-products of metal and photoresist (col. 1, line 64 - col. 2, line 1). The Ma et al. reference explains that polymer residues tend to condense into the sidewalls of the features during the etching process if not removed by the ion bombardment process (col. 2, lines 1-5). Such residue will cause a preference of ions in the nested features so that the etch residues will be thoroughly removed in contrast with isolated features thereby resulting in vertical walls in the nested features while slanted walls are present on the isolated features (col. 2, lines 6-21). The Ma et al. reference discloses a method which prevents such an undesirable "profile microloading" (col. 3, lines 24-28). In other words, the Ma et al. reference discloses a method for preventing "profile microloading" which may occur in a subsequent etching step as opposed to a previous lithographic patterning as recited by the present invention.

As explained above, in the example shown in Figs. 2A and 2B, the present invention lithographically patterns the resist pattern 203 and etches to correct the offset in the resist pattern 203. In stark contrast, as shown in Figs. 1 and 2, the Ma et al. reference does not teach or suggest any offset in the photoresist PR at all. Rather, the Ma et al. reference is concerned with preventing any offset being created by plasma etching of the gate material. Indeed, the disclosure of the Ma et al. reference is entirely directed to a "high density plasma

metal alloy etch process" (emphasis added, col. 3, lines 10-13).

Thus, the Ma et al. reference does not teach or suggest the features of the present invention including etching to compensate for an offset which was generated during a previous lithographic process. To the contrary, the Ma et al. reference does not compensate at all for any existing lithographic offset between nested and isolated features, but instead focuses on the prevention of offset which might be created during a subsequent etching.

In other words, in stark contrast to the present invention which corrects an existing offset, the Ma et al. reference discloses preventing the occurrence of an offset.

Similarly, the Horak et al. reference also does not teach or suggest etching to compensate for offset created during lithographic processing. Rather, the Horak et al. reference focuses upon preventing an offset in a subsequent etching process. Indeed, the Examiner does not allege that the Horak et al. reference remedies the deficiencies of the Tao et al. reference and the Ma et al. reference by disclosing etching to compensate for an offset created by a previousy lithographic process. Therefore, the Horak et al. reference does not teach or suggest compensating for a previous lithographically created offset.

Indeed, none of the applied references even acknowledge correcting an existing offset. Rather, the applied reference concentrate on preventing any offset which may occur from a subsequent etching. Therefore, clearly the applied references are incapable of teaching or suggesting compensating for an existing offset.

IX. CONCLUSION

Applicant requests removal of the rejection of claims 1, 3-8, 10-14 and 16-20 under 35 U.S.C. § 103(a).

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: 8/14/03

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Attachment:
Appendix

APPENDIX

Claim 1. A method of forming a semiconductor device, comprising:

lithographically patterning a structure having a first critical dimension, wherein said structure includes nested features and an isolated feature;

etching said structure with an O2-containing material to trim said first critical dimension to a second critical dimension to correct an offset between said nested features and said isolated feature created by said lithographic patterning.

Claim 3. The method of claim 1, further comprising:

forming a positive photoresist layer over a substrate prior to forming said structure in said photoresist layer.

Claim 4. The method of claim 1,

wherein said structure comprises a negative photoresist; and

wherein said etching comprises a surface charging technique in combination with a plasma etch, such that said nested feature is etched faster than said isolated feature.

Claim 5. The method of claim 1, wherein said second critical dimension is within a range of about 10-50 nm smaller than said first critical dimension.

Claim 6. The method of claim 1, wherein said etching is performed at approximately 5mT to approximately 50mT for a time of between approximately 5 seconds to approximately 40 seconds.

Claim 7. The method of claim 1, wherein said structure includes an anti-reflection coating formed on a polysilicon substrate.

Claim 8. A method of trimming a structure on a substrate, comprising:

lithographically patterning a structure having a first critical dimension, wherein said structure includes nested features and an isolated feature;

etching said structure with an O2-containing material to trim said first critical dimension to a second critical dimension, said second critical dimension being smaller than said first critical dimension to correct an offset between said nested features and said isolated feature.

Claim 10. The method of claim 8, wherein said structure comprises a positive photoresist.

Claim 11. The method of claim 8, wherein said second critical dimension is within a range of about 10-50 nm smaller than said first critical dimension.

Claim 12. The method of claim 8, wherein said etching is performed at approximately 5mT to approximately 50mT for a time of between approximately 5 seconds to approximately 40 seconds.

Claim 13. The method of claim 8, wherein said structure includes a polysilicon substrate having an anti-reflection coating formed thereon.

Claim 14. A method of etching a semiconductor device, comprising:

lithographically forming nested features and an isolated feature; and

etching said semiconductor device using a surface charging technique in combination with a plasma etch, such that a nested features formed on said semiconductor device are etched faster than an isolated feature formed on said semiconductor device to compensate for an offset between said nested features and said isolated features which resulted from said lithographic formation of said nested features and said isolated features.

Claim 16. The method of claim 14, wherein said nested features and said isolated feature comprise a negative photoresist.

Claim 17. The method of claim 14, wherein said etching uses a mixture of NF3 and argon.

Claim 18. The method of claim 14, wherein said semiconductor device includes a polysilicon substrate, a TEOS layer formed over the substrate, and an antireflection coating layer formed over the substrate.

Claim 19. A method of etching a semiconductor material, comprising:

lithographically forming nested features and an isolated feature, wherein said nested features and said isolated feature comprises a negative photoresist; and

etching said semiconductor substrate using a surface charging technique in combination with a plasma etch, such that said nested feature is etched faster than said

isolated feature to compensate for an offset between said nested features and said isolated feature created by said lithographic forming.

Claim 20. The method of claim 19, wherein said features are formed on a semiconductor substrate which comprises a polysilicon substrate, and wherein said nested features and said isolated feature comprise a TEOS layer and an antireflection coating layer.